# REMARKS

Claims 1-14 and 16-35 are pending. The Applicants' attorney has amended claims 1, 7-9, 16-18, 21-23, and 27-29, has canceled claim 15 without prejudice or disclaimer, and has added new dependent claims 30-35. All of the currently pending claims are in condition for allowance, and the Applicants' attorney requests the Examiner to withdraw all of the outstanding rejections. **But if after considering this response the Examiner does not allow all the claims, the Applicant's attorney requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

## Rejection Of Claims 28-29 Under 35 U.S.C. § 112, First Paragraph

### Claim 28

Claim 28 recites a pipeline accelerator operable to generate first pipeline data from first host data without responding to any program instruction.

Referring, e.g., to FIG. 3 and paragraph [46] of the patent application, the pipeline accelerator 44 may process data without executing program instructions.

Referring, e.g., to FIG. 3 and paragraphs [49 and [53], the pipeline accelerator 44 may include one or more programmable logic ICs (e.g., an FPGA), and thus may configure itself by downloading firmware from a memory 52; consequently, the accelerator may be hardwired to perform a data-processing operation. It is known that a hardwired data-processing circuit, such as a circuit in a handheld calculator, may process data independently of program instructions.

Referring, e.g., to FIG. 3 and paragraphs [58] – [62], the accelerator 44 may receive messages that include data but no program instructions, and thus may process this data without receiving program instructions.

Consequently, because the patent application describes at least one embodiment of the pipeline accelerator 44 that can process data without executing program instructions, independently of program instructions, and without receiving program instructions, it is inherent that the at least one embodiment may process data without responding to a program instruction.

### Claim 29

Claim 29 recites a pipeline accelerator operable to generate first pipeline data from first host data without receiving any program instruction.

Referring, e.g., to FIG. 3 and paragraphs [58] – [62], the accelerator 44 may receive messages that include data but no program instructions, and thus may process this data without receiving program instructions.

## Rejection of Claims 1-2, 5-8, 16, 28, and 29 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. 6,112,288 To Ullner

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

### Claim 1

Claim 1 as amended recites a host processor operable to execute an instruction of a program and to identify configuration information that is separate from the program, and a pipeline accelerator operable to configure a portion of itself in response to the identified configuration information.

For example, referring, *e.g.,* to FIG. 3 and paragraphs [52] - [53], an embodiment of a peer-vector machine 40 includes a host processor 42 operable to execute an instruction of a program stored in a memory 66, and operable to identify in an accelerator configuration registry 70 configuration information that is separate from the program. The peer-vector machine 40 also includes a pipeline accelerator 44 that is operable to configure a portion of itself in response to the configuration information identified by the host processor 42. For example, the host processor 42 may download the identified configuration information from the registry 70 into a firmware memory 52, and the accelerator 44 may configure itself by downloading the configuration information from the firmware memory.

In contrast, referring, *e.g.,* to Ullner's FIGS. 2, 3, and 8 and col. 8 lines 9-23, Ullner does not disclose a pipeline accelerator that is operable to configure a portion of itself in response to configuration information that is separate from a program executed by a host processor. Referring to FIG. 2, a host computer 15 executes a program having instructions. Referring to FIG. 8, an instruction decoder 78 and mode decoder 81 decode an instruction of the program to configure (via signals S0-S2) the program counter (the circuit of FIG. 8) of an accelerator chip 43 (FIG. 3). Consequently, unlike the claim 1 accelerator, which configures itself in response to information that is separate from a program executed by a host processor, Ullner's program counter configures itself in response to an instruction that is part of, and thus is not separate from, the program executed by the host computer 15.

### Claims 2 and 5-8

These claims are patentable by virtue of their dependencies from claim 1.

### Claim 16

Claim 16 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1.

### Claim 28

Claim 28 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1.

### Claim 29

Claim 29 as amended recites a host processor operable to execute a program, operable to generate in response to the executing program host data that is received by a pipeline accelerator, and, while not executing the program, operable to configure a portion of the pipeline accelerator to generate pipeline data from the host data.

For example, referring, *e.g.,* to FIG. 3 and paragraphs [52] - [53] and [55], an embodiment of a peer-vector machine 40 includes a host processor 42 that is operable to execute a program, and to generate, in response to the executing program, host data that is received and processed by a pipeline accelerator 44 (e.g., the accelerator may generate pipeline data from the host data). But while the program is not being executed by the host processor 42, (*e.g.*, before the host processor starts executing the program), the host processor may configure a portion of the pipeline accelerator 44 to receive and process the host data by providing configuration firmware from an accelerator configuration registry 70 to a firmware memory 52, from which the accelerator downloads the firmware.

In contrast, referring, *e.g.,* to Ullner's FIGS. 2, 3, and 8 and col. 8 lines 9-23, Ullner does not disclose a host processor that is operable to generate, in response to a program, host data, and that is, while not executing the program, also operable to configure a portion of the pipeline accelerator to generate pipeline data from the host data. Referring to FIG. 2, a host computer 15 executes a program having instructions and sends data generated by the program to an accelerator chip 43 (FIG. 3) for processing. Referring to FIG. 8, an instruction decoder 78 and mode decoder 81 decode an instruction of the program to configure (via signals S0-S2) the program counter (the circuit of FIG. 8) of the accelerator chip 43 to process the data sent by the host computer 15. Consequently, unlike the claim 1 host processor, which may configure a pipeline accelerator to process data generated by a program while the host processor is not executing the program, the host computer 15 can configure the accelerator 43 to process data from a program only while the host computer is executing the program. This is because the host computer 15 uses the instructions of the program itself to configure the accelerator 43.

## **Rejection of Claims 1-4, 9-12, 18, 20-21, 23, 25, 26, 28, and 29 Under 35 U.S.C. § 102(e) As Being Anticipated By U.S. 2002/0087829 To Snyder et al.**

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

**Claim 1**

Claim 1 as amended recites a host processor operable to execute an instruction of a program and to identify configuration information that is separate from the program, and a pipeline accelerator operable to configure a portion of itself in response to the identified configuration information.

In contrast, referring, *e.g.,* to Snyder's FIGS. 1-2 and 4 and paragraph [0022], Snyder does not disclose a host processor operable to execute an instruction of a program and to identify configuration information that is separate from the program, and a pipeline accelerator operable to configure a portion of itself in response to the identified configuration information. As understood by the Applicants' attorney, Snyder's sequencer 400 receives only program instructions, and thus receives no configuration information separate from the program being executed by processor that is using the complex arithmetic elements (CAEs of FIG. 2) of Snyder's scaleable functional units (SFUs) 106 (FIG. 1) to process data.

**Claims 2-4**

These claims are patentable by virtue of their dependencies from claim 1.

**Claim 9**

Claim 9 as amended recites a host processor operable to execute a program, operable to generate host data from pipeline data in response to the executing program, and, while not executing the program, operable to configure a portion of the pipeline accelerator to generate the pipeline data.

For example, referring, *e.g.,* to FIG. 3 and paragraphs [52] - [53] and [55], an embodiment of a peer-vector machine 40 includes a host processor 42 that is operable to execute a program, and to generate, in response to the executing program, host data from pipeline data that is received from a pipeline accelerator 44. But while the program is not being executed by the host processor 42, (*e.g.*, before the host processor starts executing the program), the host processor may configure a portion of the pipeline accelerator 44 to generate the pipeline data by providing configuration firmware from an accelerator configuration registry 70 to a firmware memory 52, from which the accelerator downloads the firmware.

In contrast, referring, *e.g.,* to Snyder's FIGS. 1-2 and 4 and paragraph [0022], Snyder does not disclose a host processor operable to execute a program, operable to generate host data from pipeline data in response to the executing program, and, while not executing the program, operable to configure a portion of the pipeline accelerator to generate the pipeline data. As understood by the Applicants' attorney, Snyder's sequencer 400 receives only program instructions, from which the sequencer configures other portions of the complex arithmetic element (CAE of FIG. 2), which is part of a scaleable functional unit (SFU) 106. Therefore, a host processor coupled to the SFUs can configure a CAE only while executing a program that processes data from the SFUs, and thus cannot configure a CAE during a time when the host processor is not executing this program.

### Claims 10-12

These claims are patentable by virtue of their dependencies from claim 9.

### Claim 18

Claim 18 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 9 over Snyder.

### Claims 20-21

These claims are patentable by virtue of their dependencies from claim 18.

### Claim 23

Claim 23 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Snyder.

### Claims 25-26

These claims are patentable by virtue of their dependencies from claim 23.

### Claim 28

Claim 28 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Snyder.

### Claim 29

Claim 29 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 9 over Snyder.

## Rejection of Claims 13-15, 17, 19, 22, 24, and 27 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Snyder In View Of Ullner

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

### Claims 13-15

These claims are patentable by virtue of their dependencies from claim 9.

### Claim 17

Claim 17 as amended recites a host processor operable to execute a program, operable to generate host data from pipeline data in response to the executing program, and, while not executing the program, operable to configure a portion of the pipeline accelerator to generate the pipeline data.

Per above, neither Snyder (e.g., as discussed above in conjunction with claim 9) nor Ullner (e.g., as discussed above in conjunction with claim 29) discloses or suggests a host processor operable to execute a program, operable to generate host data from pipeline data in response to the executing program, and, while not executing the program, operable to configure a portion of the pipeline accelerator to generate the pipeline data. Consequently, the combination of Snyder and Ullner does not suggest the recited subject matter.

### Claims 19 and 22

These claims are patentable by virtue of their dependencies from claim 18.

### Claims 24 and 27

These claims are patentable by virtue of their dependencies from claim 23.

## Conclusion

In light of the foregoing, claims 2-6, 10-14, 19-20, and 24-26 as previously pending, claims 1, 7, 8-9, 16-18, 21-23, and 27-29 as amended, and new claims 30-35 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are authorized to charge those fees to Deposit Account No. 50-1464.

DATED this 3rd day of August, 2007.

Respectfully Submitted,

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